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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,538	04/14/2004	Kuen-Shan Chang	06484.0223-00	4438

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,538	CHANG, KUEN-SHAN	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *8-11,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-5, 12-13, 15, 20-21, 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Aiba et al (US 2002/0190779 A1).

Aiba shows:

1. A circuit for converting voltage levels (Fig. 1, 2, or 17) comprising:

a first power supply (13) providing a first voltage level;

a second power supply providing a second voltage level (ground);

a first transistor (Q301, Fig. 17) formed between the first and second power supplies including a gate electrode for receiving an input signal including a first state (closed or low) and a second state (open or high);

a second transistor (Q12) formed between the first transistor and the second power supply including a gate electrode for receiving a bias voltage (Vb); and

a current source (I2) formed between the second transistor and the second power supply providing a current in response to the first state of the input signal;

wherein a voltage level at a node (Vg) disposed between the second transistor and the current source is pulled to a third voltage level (Vg is a predetermined potential,

col. 5, [0111]) in response to the first state of the input signal, and pulled to the second voltage level in response to the second state of the input signal (col. 5, [0107]) .

3. The circuit of claim 1, the first transistor (Q301) further comprising an electrode (source) coupled to the first power supply.

4. The circuit of claim 1, the second transistor (Q12) further comprising an electrode (source) coupled to the current source.

5. The circuit of claim 1, the bias voltage clamping the voltage level at the node between the second (groung) and third voltage levels (Vg).

12. A circuit for converting voltage levels (Fig. 1, 2, or 17) comprising;

an input signal having a first voltage level (13) and a second voltage level (ground);

a first transistor (Q301) including a gate electrode for receiving the input signal;

a second transistor (Q12) including a gate electrode for receiving a bias voltage;

a current source (I2) providing a current in response to the first voltage level of the input signal; and

a node (Vg) disposed between the second transistor and the current source;

wherein the second transistor clamps a voltage level at the node between a third voltage level (Vg) and a fourth voltage level (ground); and

wherein the voltage level at the node is approximately the third voltage level in response to the first voltage level (low or close) of the input signal, and approximately the fourth voltage level in response to the second voltage level (high or open).

13. The circuit of claim 12, the first transistor, second transistor and current source being formed between a first power supply (VDD) providing the second voltage level and a second power supply (ground) providing the fourth voltage level.

15. The circuit of claim 12, the current source further comprising a current mirror generating the current (21, fig. 2).

20, 23. the apparatus above is applicable to the method claims.

21. The method of claim 20 further comprising pulling a different voltage level at a different node (a node between Q301 and Q12) disposed between the first transistor and the second transistor in response to the first state and the second state of the input signal.

3. Claims 20, 22, 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujita (US 2003/0020516 A1).

Fujita shows:

20. A method for conveding voltage levels comprising:

providing a first power supply of a first voltage level;

providing a second power supply (ground) of a second voltage level;

forming a first transistor (M14) between the first and second power supplies including a gate electrode;

providing to the gate electrode of the first transistor an input signal (IN) including a first state and a second state;

forming a second transistor (M12) between the first transistor and the second power supply including a gate electrode;

providing to the gate electrode of the second transistor a bias voltage (Va);

forming a current source (I12) between the second transistor and the second power supply providing a current in response to the first state of the input signal;

pulling a voltage level at a node (Vb) disposed between the second transistor and the current source to a third voltage level (Vb) in response to the first state of the input signal;

and pulling the voltage level at the node to the second voltage level (ground) in response to the second state of the input signal.

22. The method of claim 20 further comprising: providing a third transistor including a gate electrode coupled to the node; and providing a fourth transistor including a gate electrode coupled to the node (inherent limitation of CMOS inverter S1).

25. The method of claim 20 further comprising providing a complementary inverter (S1).

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 2, 7, 12, 13, 16 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Prior Art (Figure 2).

1. A circuit for converting voltage levels (Fig. 2, Prior Art) comprising:

a first power supply (VDD) providing a first voltage level;

a second power supply providing a second voltage level (VEE);

a first transistor (32) formed between the first and second power supplies including a gate electrode for receiving an input signal including a first state (Vss or low) and a second state (VDD or high);

a second transistor (34) formed between the first transistor and the second power supply including a gate electrode for receiving a bias voltage (VR); and

a current source (36 and 38) formed between the second transistor and the second power supply providing a current in response to the first state of the input signal;

wherein a voltage level at a node (A) disposed between the second transistor and the current source is pulled to a third voltage level (VA=VAA) in response to the first state of the input signal, and pulled to the second voltage level in response to the second state of the input signal.

2. the first and second transistors are high-voltage transistors (page 3 [005]).

7. The circuit of claim 1 further comprising a complementary inverter (40 & 42, the output signal C is inverted from the signal A) coupled between a third power supply providing the third voltage level and the second power supply.

12-13, 16, 19 and 25. the limitations are rejected as above and the fourth voltage level is VEE.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6, 14, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aiba et al (2002/0190779 A1).

Aiba discloses the claimed invention except for the bias voltage being approximately the third or fourth voltage level plus a gate-to-source voltage of the second transistor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the bias voltage being approximately the third or fourth voltage level plus a gate-to-source voltage of the second transistor, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

Allowable Subject Matter

7. Claims 8-11, 17-18 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

6/9/05